Wafer-scale fabrication of high-aspect ratio nanochannels based on edge-lithography technique

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This paper introduced a wafer-scale fabrication approach for the preparation of nanochannels with high-aspect ratio (the ratio of the channel depth to its width). Edge lithography was used to pattern nanogaps in an aluminum film, which was functioned as deep reactive ion etching mask thereafter to form the nanochannel. Nanochannels with aspect ratio up to 172 and width down to 44 nm were successfully fabricated on a 4-inch Si wafer with width nonuniformity less than 13.6%. A microfluidic chip integrated with nanometer-sized filters was successfully fabricated by utilizing the present method for geometric-controllable nanoparticle packing. © *2012 American Institute of Physics*. [doi:10.1063/1.3683164]

INTRODUCTION

Recently, for the unique phenomena exhibited in the nanometer-sized confined space,[1] nanofluidic devices have found more and more applications in biomolecule manipulation,[2–7] transportation,[8–10] and detection.[11–14] With the development of fabrication technique, Lab-on-chip is likely to be brought into a totally new field where integrated micro/nanofluidics might play an essential role.

However, reliable fabrication of nanochannel, especially integrated with microchannel, is still a critical issue in micro/nanofluidics study. Nanolithography techniques, such as electron beam lithography (EBL),[15] focused ion beam (FIB),[16] and nanoimprint,[17] have been introduced for years to realize these high resolution nanopatterns. All the above nanolithography techniques require expensive facilities and/or very high running cost. Some techniques like FIB even fail to give a wafer-scale throughput, thereby cannot be integrated with traditional microfabrication techniques. In the past several years, wafer-scale, low-cost, and microelectromechanical system (MEMS) technique compatible nanochannel preparation has been studied, such as shallow etching-bonding method[18,19] and sacrificial layer method.[20,21] However, the above fabrication strategies only presented planar nanochannel, i.e., only the depth is at nanometer scale, which failed to provide enough processable sample volume because of the limited cross-sectional area, even in an array mode.[22] More recently, etching and filling was considered as a useful strategy for the preparation of nanochannel with a high aspect ratio, which made large sample volume operation possible.[22–24] However, a thick deposition of dielectric material, such as silicon oxide prepared by low pressure chemical vapour deposition, which was utilized to shrink the feature size, made the following channel sealing operation, usually by anodic bonding, unprocessable or with a very low yield.

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Here we presented a top-down fabrication technique for wafer-scale and high aspect ratio nanochannel preparation. Edge lithography,[25–27] a MEMS technique compatible fabrication approach, was utilized to define aluminium nanogaps, instead of chromium ones[27] due to the better etching controllability of the aluminium etchant. High aspect ratio nanochannels were then fabricated by deep reactive ion etching (DRIE) with so-prepared aluminium patterns as the etching mask. Controllability and wafer-level non-uniformity of the channel width were scrutinized. As a demonstration of the process integratibility, a microfluidic chip containing nanometer-sized filters was fabricated. Nanoparticle crystal (NPC) packing performance of this micro/nanofluidic device was preliminarily tested.

FABRICATION

The nanochannel fabrication started with a 4" ⟨100⟩ silicon wafer polished on one side and with the thickness of 510–540 μm. Firstly, the silicon wafer was coated with 80 nm aluminum by e-Beam evaporation (Nanguang ZZS550-3/D) and patterned by a standard micrometer-resolution photolithography. Masked by photoresist, the aluminum layer was isotropically etched by an aluminum etchant (H_3PO_4:HAc:HNO_3 = 16:1:1 at 39 °C; to get a repeatable etching performance, freshly prepared etchant was used in every trial) with varied etching times to generate different undercuts in the aluminum layer, as shown in Fig. 1(a). After another 80 nm thick aluminum evaporation (Fig. 1(b)), a regular lift-off process released the photoresist and left nanogaps constructed by two-step aluminum evaporation on the substrate (Fig. 1(c)). The aluminum nanogaps were then functioned as the DRIE (Multiplex ICP, Surface Technology System) etching mask for high aspect ratio nanochannels fabrication (Fig. 1(d)). The DRIE etching time varied from 5 min to 30 min with an etching/passivation cycle of 9 s/7 s. Finally, after removing the aluminum layer by etchant mentioned above, thermal oxidation further shrank the so-prepared nanochannels[28,29] and realized isolation for possible electrical measurements, as exhibited in Fig. 1(e). More importantly, this thermal oxidation step can tune the nanochannel geometrical size precisely as the silicon oxidation is a well controllable process.

To fabricate integrated micro/nanostructures on single chip, nanopatterns prepared by the above edge lithography was aligned with micro-meter patterns in a mask aligner (Karl Suss MA6/BA6) easily because nanogaps in the aluminum film were sharp enough under microscope. After transferring micropatterns onto the aluminum film, channels with width varied from nanometers to micrometers can be fabricated by DRIE simultaneously. Following this method, we have fabricated a microfluidic chip with nanometer-sized filters integrated. Briefly, nanogaps were first formed on the 80 nm aluminum layer by the above edge lithography.

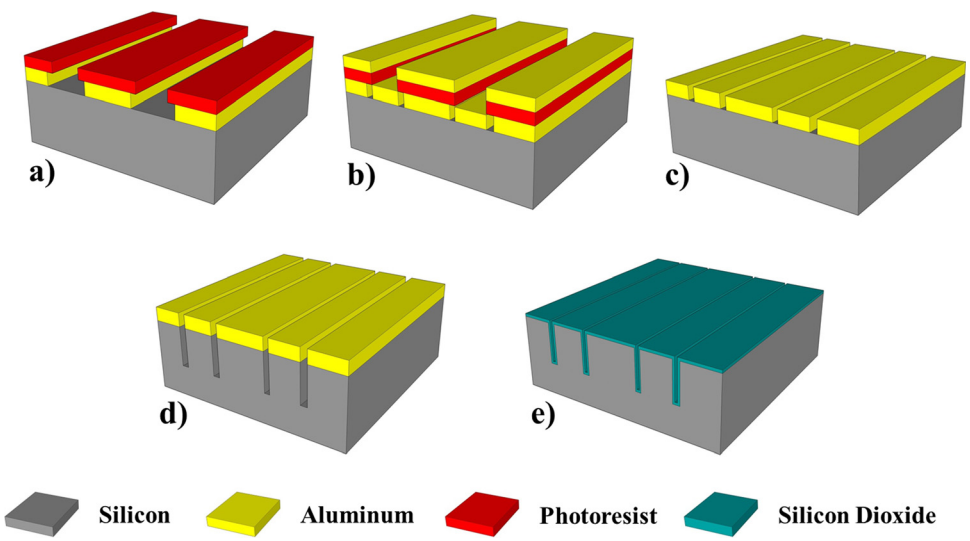

FIG. 1. Schematic illustration of the present nanochannel fabrication process.

Micropatterns were then transferred onto the aluminum layer by traditional micrometer-resolution lithography. After removing all the photoresist onside, DRIE was applied with the patterned aluminum film as the etching mask. Additional thermal oxidation was performed to precisely control the final nanochannel feature size after removing the aluminum mask. Then the chip was bonded with a glass wafer to seal the channels by anodic bonding technique. Platinum electrodes were prepared on the glass wafer in advance by a traditional lift-off approach for possible electrical measurement. The bonded wafer was then thinned from the silicon side to a suitable thickness, around 100μm, in a KOH etching bath. Finally, inlets/outlets were etched through at designed regions by DRIE.

RESULTS AND DISCUSSIONS

Width of the nanogap generated by edge lithography was tuned by varying the aluminum etching time, in the step shown in Fig. 1(a). Fig. 2 gave the relationship between the gap width and the etching time. In the present experiments, the aluminum layer was 80 nm thick, and widths of nanogaps varied from 127 ± 2 nm to 581 ± 6 nm when the corresponding etching time was set from 30 s to 110 s, where the standard deviations were calculated based on five points measured in each wafer. The linearity between nanogap width and aluminum etching time within the present work exhibited precise size controllability. For reference in the corresponding micro/nanofabrication, a nominal coefficient, which was defined as the ratio of the final nanogap width to the aluminum undercutting time, was regressed as 342 nm/min.

Nanochannels were fabricated by DRIE with the so-prepared aluminium nanogaps as the etching mask. Typical nanochannels prepared in the present work were shown in Fig. 3. In the DRIE etching, the nanochannel openings were broadened to some extents, as listed in Table I. The DRIE broaden width (nanochannel openings width minus nanogap masks width) was larger in wide starting nanogaps than that in narrow starting nanogaps. In the 11 min DRIE case, the opening widths of each set of nanochannels with undercutting time from 50 s to 110 s got increased after the DRIE, from 253 ± 6 nm to 384 ± 22 nm for the 50 s undercutting case and from 581 ± 6 nm to 934 ± 13 nm for the 110s one. Further study indicated that the broaden

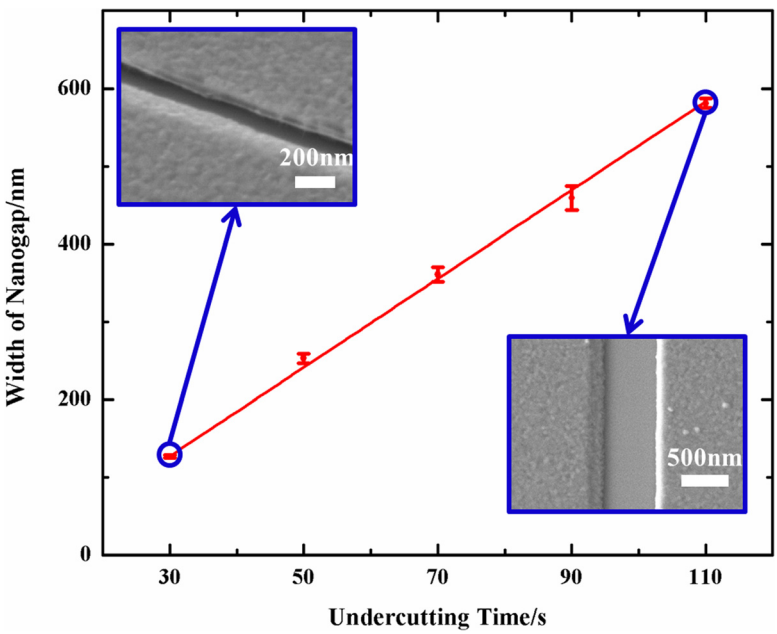

FIG. 2. Relationship between the nanogap width and the undercutting time. The error bars represent standard deviations calculated by the measurements of different locations on 4" wafer. The inserted SEM photos correspond to 30 s and 110 s undercutting cases, respectively.

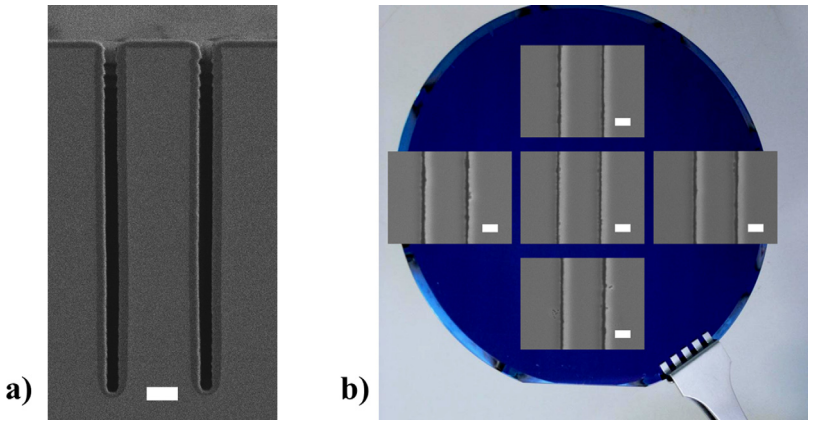

FIG. 3. (a) Typical SEM photo (cross-sectional view) of nanochannels (undercutting 50 s, DRIE 11 min, and thermal oxidization of 300 nm). The scale bar in the SEM photo is 2 μm. (b) A 4' wafer (the background photo) with nanochannels fabricated under the same fabrication condition as (a). Inserted figures are typical SEM photos (top-view) of the nanochannels at five different locations where they were taken on the wafer. The scale bars in the SEM photos are 1 μm.

width of nanochannel varied with the DRIE time, as shown in Fig. 4. The data were all collected from the case with a 50 s undercutting and 80 nm thick aluminum layer.

Fig. 5 showed the nominal etching rates of the DRIE for nanochannel fabrication, which were calculated simply by dividing the final depth of nanochannel by the DRIE time. Although the etching rate changed during the whole etching process, we can calculate the etching rate by studying the depth of nanochannel with fixed time of DRIE. Due to the LAG effect existed in DRIE, it is supposed that different etching rate should be observed in different opening cases. As demonstrated in Fig. 5, a wider nanogap has a relatively higher etching rate, the 253 nm opening nanogap got 966 nm/min nominal etching rate during DRIE process while the 581 nm opening nanogap got 1976 nm/min.

To further shrink down the nanochannel width and precisely control the final nanochannel geometrical size, the silicon wafer with nanochannels inside was thermally oxidized after removing the aluminum mask. As listed in Table I, after a 300 nm thermal oxidation (measured on top of the wafer), the nanochannel widths varied from 384 nm to 54 nm for the 50 s undercutting etching case, around a 330 nm shrinkage, which agreed quite well with theoretical calculation (324 nm, 46% of silicon should be consumed to generate 1 unit of silicon dioxide on the silicon surface during the thermal oxidization process[30]). The other three sets of statistics in Table I also showed the conformal size shrinkage by thermal oxidation. For different opening cases, a given thermal oxidation generated a consistent size shrinkage, which indicated that this posterior oxidation strategy was able to precisely control the final nanochannel size. So far, the minimum width of the nanochannels obtained after 300 nm thermal oxidation was 44 nm with an aspect-ratio of 172. In addition, thermal oxidation can reduce the edge roughness of the nanochannel sidewall because of higher oxidation rate for concave structures,[31] leading to higher width uniformity. As listed in Table I, the wafer level width non-uniformity of the present nanochannel fabrication approach was less than 13.7%, which was obtained in the 50 s

TABLE I. Opening width variation during the present fabrication and wafer-scale width non-uniformity.

Undercutting time/s	Width of aluminum nanogap/nm	DRIE time/min	Width of nanochannel/nm	Width of channel after 300 nm-thick oxidation/nm	Non-uniformity
50	253 ± 6	11	384 ± 22	54 ± 7	13.7%
70	440 ± 7	10	656 ± 50	384 ± 30	7.8%
90	458 ± 15	11	725 ± 17	495 ± 13	2.6%
110	581 ± 6	11	934 ± 13	593 ± 19	3.2%

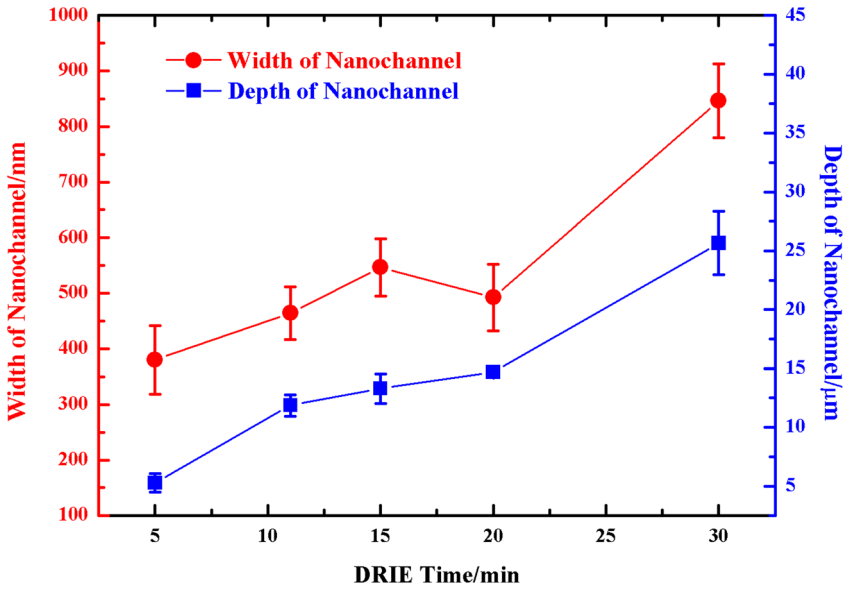

FIG. 4. Variation of the final geometrical size of the nanochannel with the DRIE time (undercutting time of 50 s). Each point in the figure stands for more than three trials.

undercutting, 11 min DRIE etching case before and after 300 nm oxidization, shown in Fig. 3. The wafer-level size uniformity granted possibility for high resolution and high throughput micro/nanofabrication integration, which can provide precise and reliable biochemical analyses on a single chip. Besides, the fabrication processes enrolled in present nanofabrication approach were all compatible with traditional MEMS techniques and made this low cost nanochannel fabrication technique promising for manufacturing micro/nanofluidic device.

As a demonstration of the process integratibility of the present technique, a microfluidic device with nano-meter sized filter integrated was fabricated. SEM photo of the so-prepared

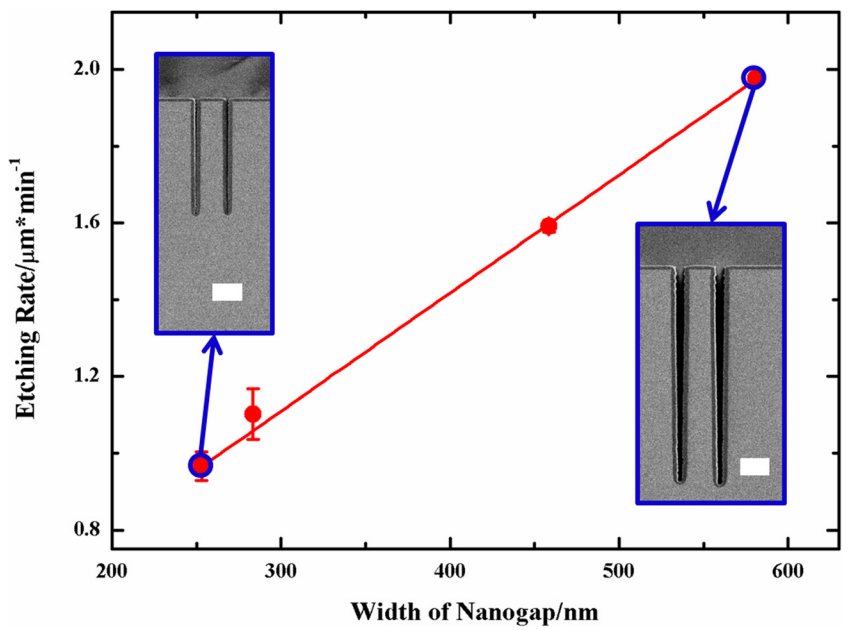

FIG. 5. Variation of the nominal DRIE etching rate with the opening width of the nanogap. Each point in the figure stands for more than three trials. The inserted SEM photos correspond to 30 s and 90 s etching cases, respectively. Both the scale bars in the SEM photos are 2 μm.

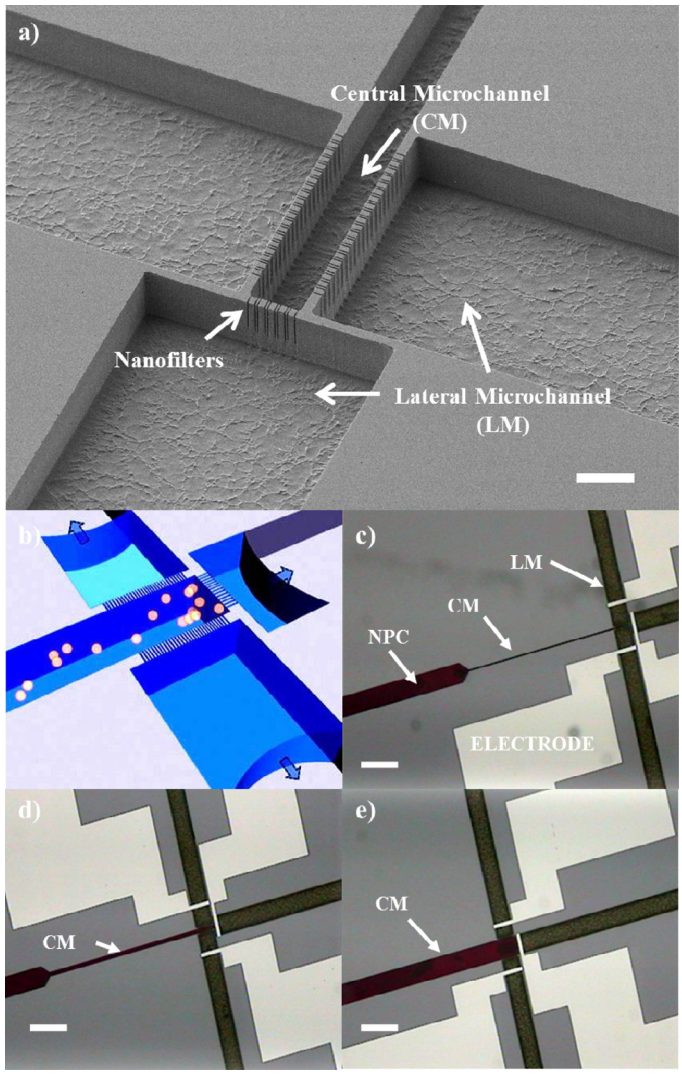

FIG. 6. Nanoparticles packing in the microfluidic chip integrated with nanometer-sized filters. (a) SEM photo of microchannel network with nanometer-sized filters. The scale bar is 10 μm. (b) Packing mechanism. The dashed blue arrows represent the evaporation direction of ethanol. (c)–(e) Packed nanoparticle crystals in the central microchannels with widths of 5, 20, and 100 μm. All the scale bars are 200 μm.

micro/nanochannels by the DRIE was showed in Fig. 6(a). The "grass-like" structure on the etched surface was caused by the DRIE, which may be overcome by using a better etching recipe. The so-etched nanochannel after DRIE was 525 nm wide. To achieve the target 450 nm-wide filter structure, a 70 nm thick oxidization was applied. In the chip, one central microchannel was connected to three lateral channels through the 450 nm-wide nanofilters, which sieved nanoparticles for the packing, as shown in Fig. 6(b). In this way, nanoparticles with different sizes or surface properties can be packed for versatile nanofluidic studies.[32,33] In our present experiment, 8 μl amino-modified 500 nm silica particles suspended in ethanol (100 mg/ml) were spotted directly at the inlet. The silica particles were drawn into the channel along with the ethanol driven by the capillary force, and then stopped by the nanofilters. Eventually, the channel was fully filled up and an optically pink nanoparticle crystal was formed after ethanol evaporation, as shown in Figs. 6(c)–6(e). By simply defining the width of the central channel, size of the packed nanoparticles between two electrodes set in the lateral channels can be accurately controlled, which will be helpful for a quantitative nanoparticle crystal based nanofluidic sensor.

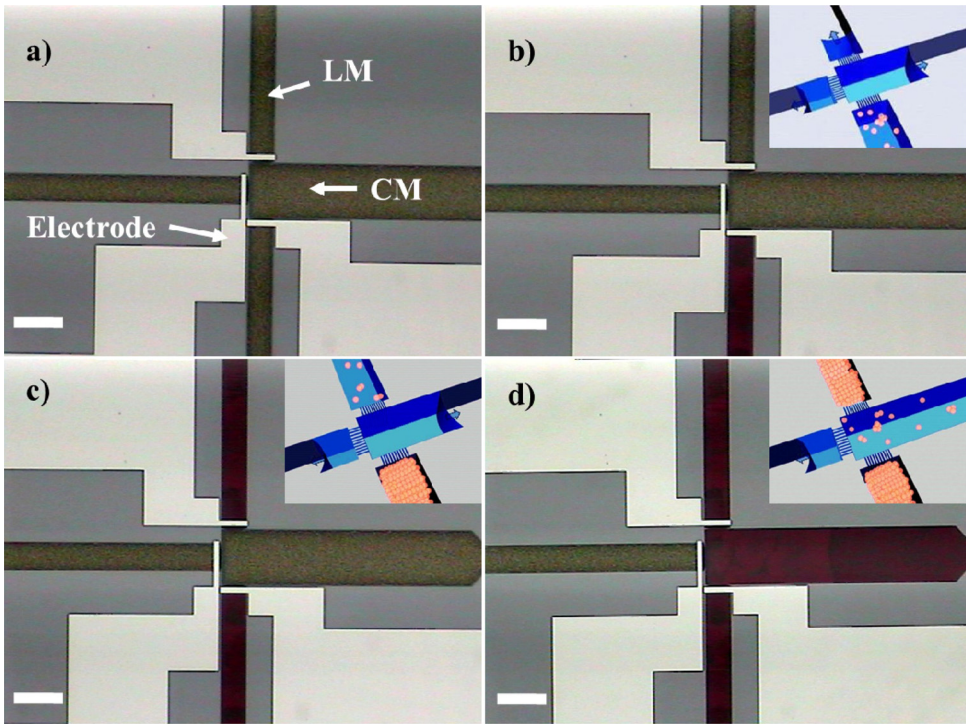

FIG. 7. Time lapse images and schematic diagrams of heterogeneous packing in connected multiple microchannels. Assembly in two opposite lateral microchannels start first, (b) and (c), and finally in the central microchannel (d). All the scale bars are 200 μm.

Except for single type nanoparticle packing, the nanofilters connecting microchannels design was also subjected to heterogeneous packing in multiple microchannels, i.e., packing nanoparticles with distinct properties in a single chip. Time lapse images were recorded to indicate the multiple-step packing process, as shown in Fig. 7. First, two lateral channels were filled up successively to let the air inside out (b)–(c), and then followed by nanoparticle assembly in the central channel (d). By this way, nanoparticles with different sizes or surface features can be packed for more powerful nanofluidic application, such as nanofluidic diode or nanofluidic transistor.

CONCLUSIONS

In this work, nanochannels with aspect ratio up to 172 and width down to 44 nm have been successfully fabricated at 4" wafer level with the width non-uniformity less than 13.7% via DRIE with edge lithographically patterned aluminum nanogaps as the etching mask. Good controllability of the geometrical sizes of the nanochannel was demonstrated and made this technique suitable for high throughput nanofabrication with a reasonable nanometer resolution. Easy to be integrated with traditional MEMS techniques also granted this approach possibility for micro-nanochannel integration. Based on the preliminary micro/nanofabrication results, the present nanofabrication technique showed great capability in various micro/nanofluidic systems.

ACKNOWLEDGMENTS

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